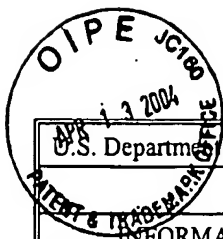


U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-12200-1D US		Unassigned <u>10/658934</u>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)			
(Use several sheets if necessary)				Chia-Shun Hsiao			
				Filing Date		Group	
				Herewith		Unassigned	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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							Translation
		Document	Date	Country	Class	Subclass	Yes No
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<u>A.M</u>	AO	Aritome, S. et al. "A 0.67 μ m ² Self-Aligned Shallow Trench Isolation Cell (SA-STI Cell For 3V-only 256Mbit NAND EEPROMs," International Electron Devices meeting 1994, San Francisco, CA December 11-14, 1994, pages 94-61 - 94-64.					
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	AR	United States Patent Application No. 10/262,785, entitled "Floating Gate Memory Fabrication Methods Comprising A Field Dielectric Etch With A Horizontal Etch Component," filed on October 1, 2002, Inventor: Yi Ding, Attorney Docket No.: M-12841 US.					
Examiner <u>ANH D. MAI</u>		Date Considered <u>11/16/04</u>					
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(Use several sheets if necessary)					Chia-Shun Hsiao			
					Filing Date		Group	
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
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(Use several sheets if necessary)					Chia-Shun Hsiao			
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		Document	Date	Country	Class	Subclass	Translation	
							Yes	No
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